Claim 13 claims a semiconductor device in claim 19 claims a method of manufacturing a semiconductor device. In particular, an active area has a recess defined by first, second and third edges while the active area has a fourth edge. A first gate electrode has a first end which extends beyond the fourth edge over an insulating film. A second gate electrode has a first end which extends beyond the third edge over the insulating film. The first gate electrode has a first length from the fourth edge to the first end thereof. The second gate electrode has a second length from the third edge to the first end thereof. The second length is greater than the first length.

Through the structure and method of the claimed invention having the length of the second gate electrode, which extends beyond the third edge, being greater than the length of the first gate electrode which extends beyond the fourth edge, as claimed in claims 13 and 19, the claimed invention provides a semiconductor device and method of manufacturing thereof which prevents occurrence of current leakage between source/drain regions which are formed on the exterior of the gate electrodes. The prior art does not show, teach or suggest the difference in lengths between the gate electrodes as claimed in claims 13 and 19.

Claims 13, 17-19, 23 and 24 were rejected under 35 U.S.C. § 103 is being unpatentable over *Shou et al.* (U. S. Patent No. 5,811,859) in view of *Bergemont* (WO 94/29898).

Applicant's respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for

reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Shou et al. appears to disclose in FIG. 3, a LSI pattern of inverted amplifier INV consisting of 3 stages MOS inverters, I1, I2 and I3. For the inverters I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. P-type semiconductor layer PL2 and N-type semiconductor layer NL2 are shaped for I3. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. A contact is a metal part passing through in semiconductor layer in the direction of thickness, for electrical connection. The drain voltage Vdd and source voltage Vss are connected to PL2 and NL2 through contacts C7 and C8. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for an output from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. The semiconductor layers PL2 and NL2 are provided with contacts C9 and C10 for an output from the third stage, respectively, from which an output is introduced through a poly-silicon portion PS toward the next stage. A strangulation portion S1 is provided between the contacts C1 and C5 in the semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. A strangulation portion S2 is provided between contacts C7 and C9 in the semiconductor layers PL2, and a strangulation portion S4 is provided between contacts C8 and C10 in the semiconductor layer NL2. These strangulation means S1 and S3 limit an electric current of the output of inverter I2, and it simultaneously

decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency. (col. 2, line 44 through col. 3, line 8)

Thus, *Shou et al.* merely discloses two gates formed within semiconductor layers PL1 and NL1. It is clearly shown in Figure 3 of *Shou et al*, the lengths of the two gate electrodes are equal and in addition only one gate electrode extends over the strangulation S1. Thus, nothing in *Shou et al.* shows, teaches or suggests a) that both the first and second gate electrodes extend beyond the third and fourth edges of the active area and b) that the length of the second gate electrode extending beyond the third edge is greater than the length of the first gate electrode extending beyond the fourth edge as claimed in claims 13 and 19. Rather, *Shou et al.* clearly discloses that the lengths of the gate electrodes are equal and that only one of the gate electrodes extends beyond the edge of the strangulation S1.

Bergemont appears to disclose, according to conventional single poly integrated circuit fabrication techniques, all of the polysilicon lines in the circuit are defined simultaneously utilizing a single mask step. That is, a layer of polysilicon (poly1) is first formed over the entire device structure. A poly 1 photoresist mask is then formed and pattern to define the underlying polysilicon. A single etch step is then performed to define individual poly1 lines. As shown in Fig. 1A, the fabrication process specification defines the desired offset distances "a" and "b" for the "end caps" of the individual polysilicon lines in both the x-direction and the y-direction, respectively. However, rather than the substantially rectangular (90^0) geometry shown in Fig. 1A, in reality, the final geometry of both the field oxide island 10 and the end cap of the polysilicon line 12 is more "rounded",

as shown in Fig. 1B. The field oxide rounding effect is inherent to the type of field isolation and photolithographic process used. The poly end cap rounding effect is inherent to the photolithography of small polysilicon lines. As shown in Fig. 1B, these physical rounding effects result in a reduced width of the polysilicon lines 10 at the poly1/field oxide interface. Thus, when the poly1 line is used as a self-aligned mask for the implementation of dopant to create the source and drain regions of MOS transistors in the circuit, the channel length of the MOS device is reduced, leading to undesirable current leakage from one side of the poly1 to the other. Any misalignment of the poly1 mask further exacerbates this leakage problem, as shown in Fig. 1C. To avoid this problem, prior art techniques rely on larger design rules. That is, design rules for the length of the poly end cap, the distance between the poly end cap and the parallel edge of the field oxide, and the width of the poly1 line all may be increased. These steps insure that the channel length of each of the MOS devices in the circuit is greater than an acceptable minimum required to prevent leakage.

Thus, *Bergemont* merely discloses offset distances for the end caps which are rounded. Nothing in *Bergemont* shows, teaches or suggests that the length of the second gate electrode extending beyond the third edge is greater than the length of the first gate electrode extending beyond the fourth edge as claimed in claims 13 and 19. Rather, *Bergemont* merely discloses offset distances for rounded end caps.

Since nothing in *Shou et al.* or *Bergemont* shows, teaches or suggests the difference in lengths of the gate electrodes extending beyond the edges of the active region as claimed

in claims 13 and 19, it is respectfully requested that the Examiner withdraws the rejection to claims 13 and 19 under 35 U.S.C. §103.

Claims 17-18, 23-24 depend from claims 13 and 19 and recite additional features. It is respectfully submitted that claims 17-18 and 23-24 would not have obvious within the meaning of 35 U.S.C. §103 over *Shou et al.* and *Bergemont* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 17-18 and 23-24 under 35 U.S.C. §103.

Claims 14-16 and 20-23 were rejected under 35 U.S.C. §103 as being unpatentable over *Shou et al.* and *Bergemont* and further in view of *Jassowski et al.* (U.S. Patent No. 5,668,389).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejections to the claims and allows the claims to issue.

As discussed above, since nothing in *Shou et al.* or *Bergemont* show, teach or suggest the primary features of the claimed invention, it is respectfully submitted that the combination of the primary references with the secondary reference of *Jassowski et al.* will not overcome the deficiencies thereof. Furthermore, even though the Examiner indicated in Fig. 2 of *Jassowski et al.* gates and edges, nothing corresponds to the structure that "the length of the second gate electrode beyond the third edge is greater than the length of the first gate electrode beyond the fourth edge" when looking at a third edge E3 and a fourth edge E4 labeled by the Examiner. Applicants respectfully submit that the Examiner's view

is speculative. Moreover, the Examiner specifies edge E5 and states that gate G1 is disposed so closely to the edge E5 that the gate length is set at a length of E5 plus the length of the margin of gate G2. However, claims 13 and 19 are not directed to the pattern of the portion where gate G1 is but are directed to the pattern having a concave part defined by edges E1, E2 and E3. Applicants respectfully submit that citing an irrelevant edge E5 and gate G1 is improper. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 14-16 and 20-23 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is now in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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